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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/692,255

10/22/2003

Terry Lines

100-14310 (P04927-C1)

9418

33402

7590

09/07/2004

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EXAMINER

LEE, EUGENE

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/692,255

**Applicant(s)**

LINES, TERRY

**Examiner**

Eugene Lee

**Art Unit**

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/22/03.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 thru 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the second semiconductor material" in line 20 of said claim. There is insufficient antecedent basis for this limitation in the claim.

It is unclear whether the applicant is referring to "a second semiconductor region" in line 16 or a different structure. Appropriate clarification and correction are required.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein 4,205,330 in view of Nagata et al. 4,015,281. Klein discloses (see, for example, Fig \_4) a MOSFET circuit (semiconductor circuit) comprising a depletion mode device (first transistor) wherein the depletion mode device comprises a first semiconductor region, source 37, drain 38, region (first channel) 30a, first gate oxide 29a, and gate 34; an enhancement device (second

Art Unit: 2815

transistor) wherein the enhancement device comprises a second semiconductor region, source 35, drain 36, region (second channel) 30, second gate oxide 29, and gate 32.

Klein does not disclose the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide. However, Nagata discloses (see, for example, FIG. 9) a semiconductor device comprising a depletion-type transistor with a gate electrode 51 and an enhancement-type transistor with a gate electrode 48. The depletion-type transistor comprises a SiO<sub>2</sub> layer (first gate oxide) 37 and the enhancement-type transistor comprises a double oxide layer wherein the double layer comprises Al<sub>2</sub>O<sub>3</sub> (aluminum oxide) layer 37 and SiO<sub>2</sub> layer 38. The SiO<sub>2</sub> layer of the depletion-type transistor is less thick than the double oxide layer oxide of the enhancement-type transistor. In column 6, lines 62-68, Nagata discloses the double layer is suitably controlled to cancel the holes existing in the surface portion of a semiconductor substrate so as to thereby easily control the gate voltage or threshold voltage. In column 8, lines 29-33, Nagata further discloses the depletion type transistor and enhancement type transistor having optimum threshold voltages while eliminating the formation of a parasitic transistor. Therefore, it would have been obvious to one of ordinary skill in the art to have the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide in order to easily control the gate voltage or optimize the threshold voltage (while eliminating the formation of a parasitic transistor).

Regarding the limitation “the first channel having a first dopant concentration” and the limitation “the second channel having a second dopant concentration”, see column 4, lines 7-11 wherein Klein discloses phosphorous, an n-type impurity, implanted to create the phosphorous doped region 30a, 30.

Regarding the limitation “the first transistor conducting more than leakage current when the gate, the source, and the first semiconductor region are connected to a same potential (which is a depletion device according to applicant’s specification on page 1)” and the limitation “the second transistor being substantially non-conductive when the gate of the second transistor, the source of the second transistor, and the second semiconductor region are connected to a same potential (enhancement device)”, see, for example, column 4, lines 10-11 wherein Klein discloses the depletion mode device with region 30a and the enhancement device with region 30.

Regarding the limitation “the first channel length being approximately 30 percent to 80 percent as long as the second channel length”, Klein discloses the first channel length being less than the second channel length, however, Klein does not disclose the first channel length being approximately 30 percent to 80 percent as long as the second channel length. However, the length of the first channel and second channel and their lengths relative to each other are result effective variables that one of ordinary skill in the art would optimize to maximize the operation of the depletion and enhancement device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the first channel length being approximately 30 percent to 80 percent as long as the second channel length, in order to maximize the performance between the depletion type device and enhancement device, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 2, see, for example, column 4, lines 11-18, wherein Klein discloses the phosphorus implant at 30 will only have a small effect in the region of the enhancement type

Art Unit: 2815

device and the region 30a of the depletion type device will produce a junction and an n-type surface channel which is more heavily doped than the substrate.

***Allowable Subject Matter***

5. Claims 3 thru 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

**INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/692,255  
Art Unit: 2815

Page 6

Eugene Lee  
September 1, 2004

A handwritten signature in black ink, appearing to read 'Eugene Lee', with a stylized, flowing script.